REMARKS

Applicant appreciates the continued thorough examination of the present application that is reflected in the second non-final Official Action of February 2, 2006. However, Applicant respectfully requests reconsideration of the new rejection of Claim 1 based on the combination of three references: U.S. Patent 6,632,718 to Grider et al. (previously cited), in view of the Wolf et al. textbook Page 834 (previously cited) and in further view of the Wolf textbook Pages 308-309 (newly cited). Respectfully, the Official Action is now attempting to use a combination of three references to teach these relatively straightforward recitations of Claim 1:

> ...wherein the first impurity region has higher impurity concentration than the second impurity region; and
>
> wherein the fourth impurity region has impurity concentration as high as the third impurity region.

Respectfully, the very use of snippets of three references in an attempt to teach these relatively straightforward recitations proves that Claim 1 is unobvious. Moreover, as will be described below, the above recitations are simply not taught by the combination of these references.

Specifically, the Official Action concedes at Page 3 that:

> Grider et al. does not teach that the fourth impurity region has impurity concentration as high as the third impurity region.

In an attempt to supply the missing teaching, the Official Action continues to cite Wolf et al. As was described at length in Applicant's last Amendment of November 18, 2005, the cited passages from Wolf et al. teach doping the source/drain extensions of both the NMOS and the PMOS devices with the same concentration as the respective source/drains (S/D). Accordingly, if Wolf et al. was substituted into Grider et al., then the claimed first impurity region would have impurity concentration as high as the second impurity region, and the fourth impurity region would have impurity concentration as high as the third impurity region. The Examiner has now agreed with this analysis because Page 3 of the Official Action states:

> Although in the above-quoted section, Wolf et al. appears to teach giving the first impurity region an impurity concentration as high as the second impurity region...

The present Official Action now adds yet a third reference, which is another paragraph from an earlier Wolf textbook, and states:

> ...Wolf additionally teaches that is beneficial in PMOS structures to have a lightly-doped LDD tip region shallower than the heavily doped p+ source/drain region to limit punchthrough (vol. 3, paragraph bridging pp. 308-309).

However, the reasonable consequence of combining Wolf (lightly-doped tip region in PMOS structures) with Wolf et al. (same impurity concentrations for PMOS and NMOS) would be to have lightly-doped tip regions in both the PMOS and NMOS devices. This is, of course, contrary to the recitations of Claim 1 quoted above.

The above analysis also clearly shows the futility of combining a primary reference with two paragraphs from two different secondary references, in an attempt to build the claimed invention. Stated differently, the primary reference Grider et al. teaches the use of lightly-doped source/drain extensions for both NMOS and PMOS devices. The secondary reference Wolf et al. teaches source/drain extensions of both the NMOS and the PMOS devices with the same concentration as the respective source/drains. The new tertiary reference to Wolf teaches that lightly-doped drain extensions may be useful in PMOS devices. This combination of three teachings simply does not describe or suggest the above-quoted recitations of Claim 1, unless one selectively chooses the teachings with the idea of building Claim 1 in hindsight.

Applicant respectfully submits that, to establish a *prima facie* case of obviousness, the prior art references when combined must teach or suggest all the recitations of the claims, and there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine reference teachings. *See* M.P.E.P. § 2143. The mere fact that references can be combined does not render the resultant combination obvious unless the prior art ***also suggests the desirability of the combination***. *See* M.P.E.P. §2143.01(citing *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990)). As emphasized by the Court of Appeals for the Federal Circuit, to support combining references, evidence of a suggestion, teaching, or motivation to combine must be ***clear and particular***, and this requirement for clear and particular evidence is not met by broad and conclusory statements about the teachings of references. *In re Dembiczak*, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). In another decision, the Court of Appeals for the Federal Circuit has stated that, to support combining or modifying references, there must be

particular evidence from the prior art as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed. *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

Respectfully, the "motivation" cited by the Official Action at Page 4, first full paragraph, does not provide the clear and particular motivation that is required by the M.P.E.P. and the case law. In particular, the Official Action states:

> The motivation at the time of the invention for giving the fourth impurity region an impurity concentration as high as the third impurity region would have been to fabricate a deep submicron FET, using ion implantation to form the source/drain extensions, as expressly taught by Wolf et al. The motivation for leaving the first impurity region with a high impurity concentration than the second impurity region would be to limit punchthrough in the PMOS device, as expressly taught by Wolf.

Applicant respectfully submits that fabricating deep submicron FETs with extension regions is a general motivation for all integrated circuit FETs and is not the clear and particular motivation that is required by the case law and the courts. Similarly, limiting punchthrough in a PMOS device is also a general motivation for all integrated circuit FETs and is not the clear and particular motivation that is required by the case law and the courts. Finally, the very next paragraph of Wolf et al. (Page 309) clearly states that lightly-doped drain structures can also be used in NMOS devices:

> Adding an LDD structure to a PMOS device in CMOS involves relatively straightforward changes in the process sequence. The gate sidewall spacers are already available from the creation of NMOS LDDs, but there is some increase in process complexity, (especially if the former process used a maskless n^- implant to form the tip regions of the NMOS LDD). That is, to form both PMOS and NMOS LDDs four masking steps are generally needed (n^-, p^-, n^+, p^+), rather than just two. However, a two-mask process, which employs removable polysilicon spacers, has also been reported. (Emphasis added.)

Accordingly, the Wolf reference does not teach only adding lightly-doped regions to the PMOS devices, but teaches adding them to the NMOS devices as well. As such, the "teaching" ascribed to Wolf at Page 3 of the Official Action as quoted above:

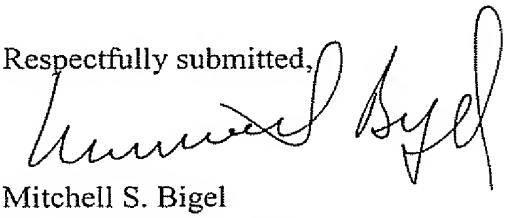
> ...Wolf additionally teaches that is beneficial in PMOS structures to have a lightly-doped LDD tip region shallower than the heavily doped p+ source/drain region to limit punchthrough (vol. 3, paragraph bridging pp. 308-309),

is not even supported by the actual teaching of Wolf. The actual teaching of Wolf is to provide lightly-doped LDD tip regions in both NMOS and PMOS devices, contrary to the recitations of Claim 1.

For at least these reasons, Claim 1 is patentable over Grider et al. in view of Wolf et al. and in further view of Wolf. Remaining dependent Claims 4-8 are patentable at least per the patentability of Claim 1 from which they depend.

In conclusion, Applicant appreciates the continued thorough examination by the Examiner. However, in view of the above analysis, Applicant respectfully submits that the pending claims are patentable over Grider et al. in view of Wolf et al. in further view of Wolf. Accordingly, Applicant respectfully requests allowance of the present application and passing the application to issue.

Respectfully submitted,



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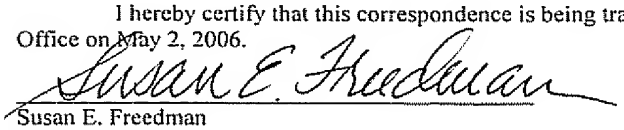

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Date of Signature: May 2, 2006